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CS 200 Project 2

February 8, 2017

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Project 2 – BCD and Modulo-10

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**Purpose:**

The purpose of this project is to make two different types of circuits. The first one is a BCD to 7 segment display. This circuit is to have 4 inputs and 7 columns of output. This circuit does not need to account for any number above the number 9 because the counter will never give anything outside of 0 to 9. We can assume that 10 to 15 will not affect the display. The next circuit is a modulo-10 counter that uses JK Flip-flops. JK flip-flops have two input pins on the bottom that will allow us to reset the value at a specific number. A way to reset the count at 9, is to use these pins to reset the count.

**Research:**

This project is worded quite difficult. As mentioned in the requirements there is an example schematic of a Modulo-16 counter on page 142 in the textbook. There are also plenty of examples of modulo counters online. To name a few:  
  
<http://www.learningelectronics.net/worksheets/counters.html>

<http://courses.cs.vt.edu/~cs2505/fall2011/Notes/T33_Counters.pdf>

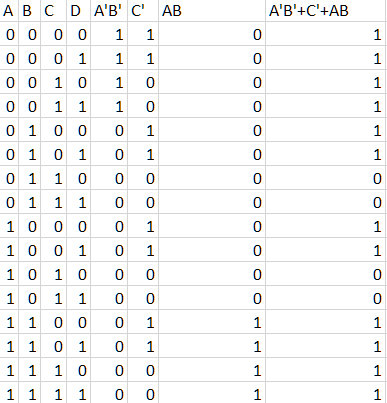
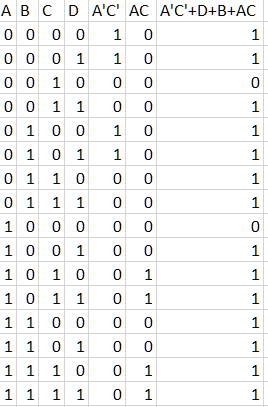
<http://www.electronics-tutorials.ws/sequential/seq_2.html>

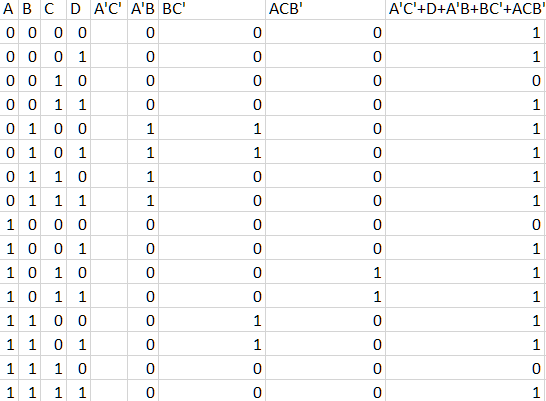
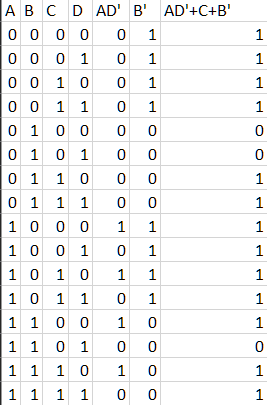
These three websites helped to give me a basic understanding of counters and how JK flip flops reset. To add on to this, friends helped me understand the issues I had with the wording of the project. A video on BCD to 7 segment displayed came up with this: <https://www.youtube.com/watch?v=2n7nM001Oi4>

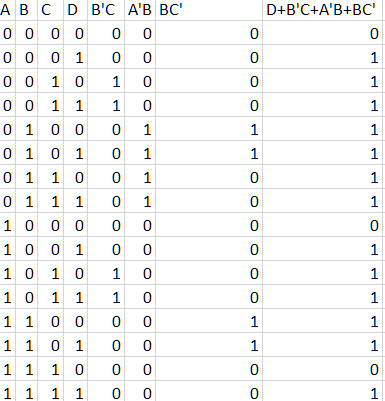
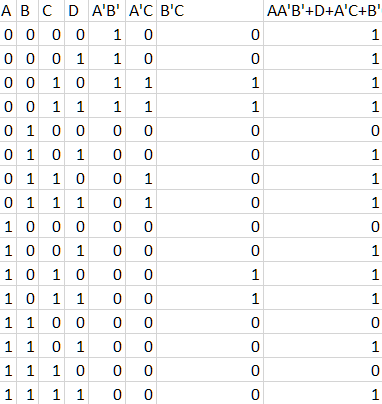
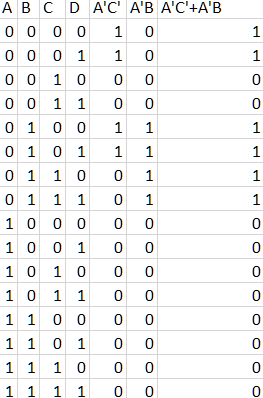
This video is a helpful demonstration of what is required for the project. The downside is that this was filmed using a different program and not Logisim.

**Truth Tables:**

Here are the many truth tables for this project. It was a bit confusing to compile them into one large truth table, so they are separated into 7 different truth tables. These truth tables show the outputs for the BCD.







**K-Maps:**

Below are the various K-maps for the above truth tables. These K-maps all contain 4 variables and are of the minimized function. Creating these K-maps was quite time consuming but verified the circuit in logisim.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | cd |  |  |  |  |
| ab |  | 00 | 01 | 11 | 10 |
|  | 00 | 1 | 1 | 1 | 0 |
|  | 01 | 1 | 1 | 1 | 1 |
|  | 11 | 1 | 1 | 1 | 1 |
|  | 10 | 0 | 1 | 1 | 1 |

F(a,b,c,d) = A’C’+D+B+AC

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | cd |  |  |  |  |
| ab |  | 00 | 01 | 11 | 10 |
|  | 00 | 1 | 1 | 1 | 1 |
|  | 01 | 1 | 1 | 0 | 0 |
|  | 11 | 1 | 1 | 1 | 1 |
|  | 10 | 1 | 1 | 0 | 0 |

F(a,b,c,d) = A’B’+C’+AB

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | cd |  |  |  |  |
| ab |  | 00 | 01 | 11 | 10 |
|  | 00 | 1 | 1 | 1 | 1 |
|  | 01 | 0 | 0 | 1 | 1 |
|  | 11 | 1 | 0 | 1 | 1 |
|  | 10 | 1 | 1 | 1 | 1 |

F(a,b,c,d) = B’+C+AD’

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | cd |  |  |  |  |
| ab |  | 00 | 01 | 11 | 10 |
|  | 00 | 1 | 1 | 1 | 0 |
|  | 01 | 1 | 1 | 1 | 1 |
|  | 11 | 1 | 1 | 1 | 0 |
|  | 10 | 0 | 1 | 1 | 1  D |

F(a,b,c,d) = A’C’+D+A’B+BC’+AB’C

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | cd |  |  |  |  |
| ab |  | 00 | 01 | 11 | 10 |
|  | 00 | 1 | 1 | 0 | 0 |
|  | 01 | 1 | 1 | 1 | 1 |
|  | 11 | 0 | 0 | 0 | 0 |
|  | 10 | 0 | 0 | 0 | 0 |

F(a,b,c,d) = A’C’+A’B

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | cd |  |  |  |  |
| ab |  | 00 | 01 | 11 | 10 |
|  | 00 | 1 | 1 | 1 | 1 |
|  | 01 | 0 | 1 | 1 | 1 |
|  | 11 | 0 | 1 | 1 | 0 |
|  | 10 | 0 | 1 | 1 | 1  D |

F(a,b,c,d) = A’B’+D+A’C+B’C

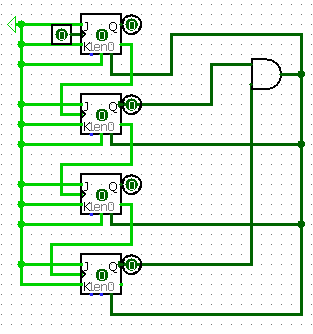
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | cd |  |  |  |  |
| ab |  | 00 | 01 | 11 | 10 |
|  | 00 | 0 | 1 | 1 | 1 |
|  | 01 | 1 | 1 | 1 | 1 |
|  | 11 | 1 | 1 | 1 | 0 |
|  | 10 | 0 | 1 | 1 | 1 |

F(a,b,c,d) = D+B’C+A’B+BC’

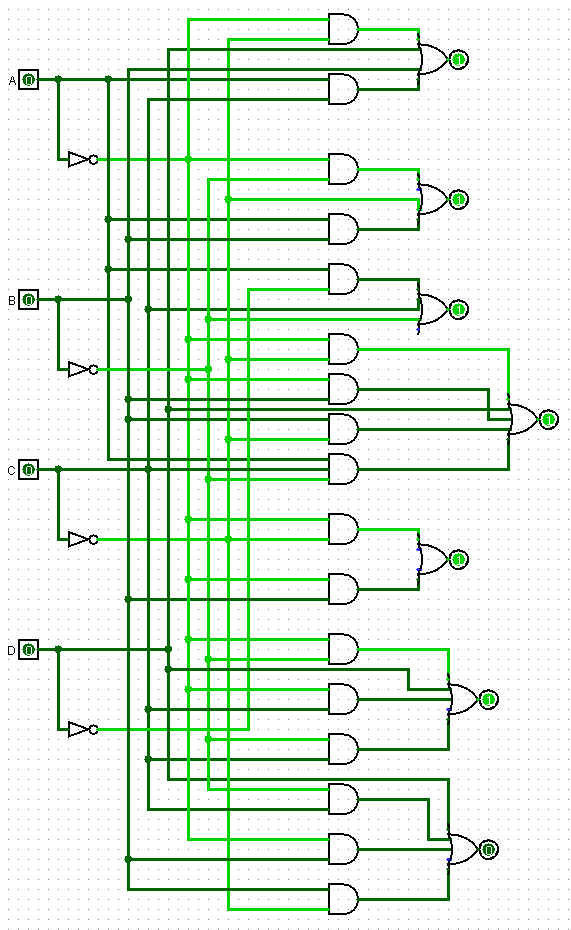
**Logisim Circuit:**

Below are the two circuits required for the 7-segment display counter. They include the BCD and the JK flip-flop counter. I attempted to make them as clean and compact as possible but that resulted in some errors. These circuits functioned properly and are quite easy to follow along.

JK Flip-Flop Counter/Modulo-10 Counter:

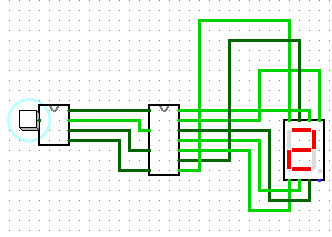
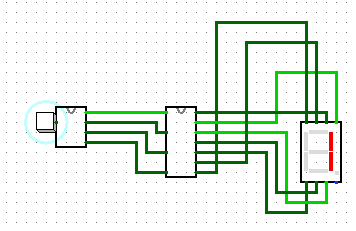
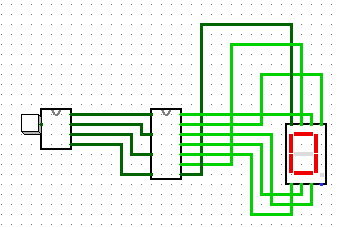


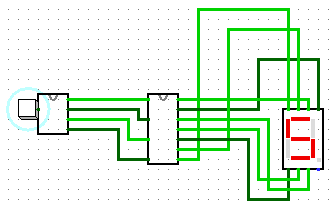
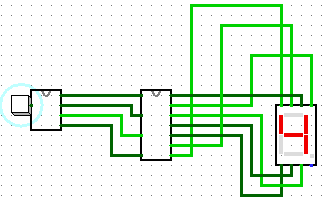
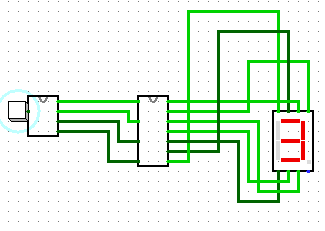
BCD:

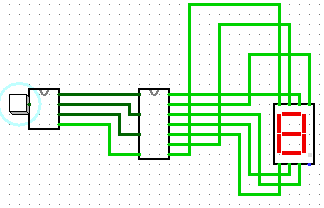
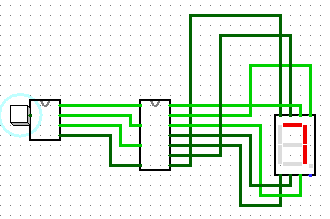
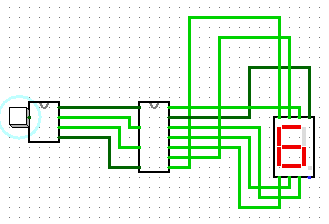


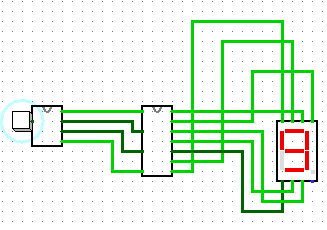
Main:

Here are the 10 outcomes of the circuit. This shows it functions and displays the number correctly.









The button was replaced with a clock afterwards. The button was used for troubleshooting and testing purposes.

**Conclusion:**

Overall this was a very insightful lab for me. It taught me a lot about J-K flip flops. I had no idea that they had reset pins at the bottom of them. This project would have been much more difficult without the resources available to me. All the information on counters and BCDs helped greatly during this project. The clarification of instructions by my friends in the class, also assisted in me finishing this project. The amount of truth tables and K-maps used during this project also honed my skills in creating them. I am much more confident in my skills at Logisim as well. Drawing circuits within Logisim is entertaining and fun. I learned that you can set the size of gates, making them look sleek and orderly. The circuits as they are now function properly and solve the problem given to me by the project outline. I am quite happy with the circuits and do not see much room for improving them.